

CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claims(s):

1. (Currently Amended) A data processor comprising:

an instruction execution pipeline comprising N processing stages capable of executing a load instruction;

a status register capable of storing a modifiable configuration value, said modifiable configuration value having a first value indicating said data processor is capable of executing a misaligned access handling routine and a second value indicating said data processor is not capable of executing a misaligned access handling routine;

a misalignment detection circuit capable of determining if said load instruction performs a misaligned access to a target address of said load instruction and, in response to a determination that said load instruction does perform a misaligned access, generating a misalignment flag;

a data protection unit capable of determining if said load instruction access a restricted area of memory and, in response to a determination that said load instruction accesses a restricted area of memory, determining if said load instruction is speculative; and

exception control circuitry capable of detecting said misalignment flag and in response thereto determining if said modifiable configuration value is equal to said first value, wherein said exception control circuitry is further capable of, in response to a determination that said load instruction is speculative, causing said data processor to dismiss said load instruction.

2. (Original) The data processor as set forth in Claim 1 wherein said exception control circuitry, in response to a determination that said modifiable configuration value is equal to said first value, causes said data processor to execute said misaligned access handling routine.

3. (Original) The data processor as set forth in Claim 1 wherein said exception control circuitry, in response to a determination that said modifiable configuration value is equal to said second value, determines if said load instruction is speculative.

4. (Original) The data processor as set forth in Claim 1 wherein said exception control circuitry, in response to a determination that said load instruction is speculative, causes said data processor to dismiss said load instruction.

5. (Canceled).

6. (Currently Amended) The data processor as set forth in ~~Claim 5~~ Claim 1 wherein said

data protection unit, in response to a determination that said load instruction does access a restricted area of memory and in response to a determination that said load instruction is not speculative, causes said data processor to execute an exception handling routine.

7. (Canceled).

8. (Canceled).

9. (Currently Amended) A processing system comprising:

a data processor;

a memory coupled to said data processor;

a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor, said data processor comprising:

an instruction execution pipeline comprising N processing stages capable of executing a load instruction;

a status register capable of storing a modifiable configuration value, said modifiable configuration value having a first value indicating said data processor is capable of executing a misaligned access handling routine and a second value indicating said data processor is not capable of executing a misaligned access handling routine;

a misalignment detection circuit capable of determining if said load instruction performs a misaligned access to a target address of said load instruction and, in response to a determination that said load instruction does perform a misaligned access, generating a misalignment flag;

a data protection unit capable of determining if said load instruction access a restricted area of memory and, in response to a determination that said load instruction accesses a restricted area of memory, determining if said load instruction is speculative; and

exception control circuitry capable of detecting said misalignment flag and in response thereto determining if said modifiable configuration value is equal to said first value, wherein said exception control circuitry is further capable of, in response to a determination that said load instruction is speculative, causing said data processor to dismiss said load instruction.

10. (Original) The processing system as set forth in Claim 9 wherein said exception control circuitry, in response to a determination that said modifiable configuration value is equal to said first value, causes said data processor to execute said misaligned access handling routine.

11. (Original) The processing system as set forth in Claim 10 wherein said exception control circuitry, in response to a determination that said modifiable configuration value is equal to said second value, determines if said load instruction is speculative.

12. (Original) The processing system as set forth in Claim 11 wherein said exception control circuitry, in response to a determination that said load instruction is speculative, causes said data processor to dismiss said load instruction.

13. (Canceled).

14. (Currently Amended) The processing system as set forth in ~~Claim 13~~ Claim 9 wherein said data protection unit, in response to a determination that said load instruction does access a restricted area of memory and in response to a determination that said load instruction is not speculative, causes said data processor to execute an exception handling routine.

15. (Canceled).

16. (Canceled).

17. (Currently Amended) For use in a data processor comprising: 1) an instruction execution pipeline comprising N processing stages capable of executing a load instruction and 2) a status register capable of storing a modifiable configuration value, the modifiable configuration value having a first value indicating the data processor is capable of executing a misaligned access handling routine and a second value indicating the data processor is not capable of executing a misaligned access handling routine, a method of handling exceptions in the data processor comprising the steps of:

determining if said load instruction access a restricted area of memory;

in response to a determination that said load instruction accesses a restricted area of memory, determining if said load instruction is speculative;

in response to a determination that said load instruction accesses a restricted area of memory and is speculative, causing said data processor to dismiss said load instruction;

in response to a determination that said load instruction does not access a restricted area of memory, determining if the load instruction is performing a misaligned access to a target address of the load instruction;

in response to a determination that the load instruction is performing a misaligned access, generating a misalignment flag; and

detecting the misalignment flag and in response thereto determining if the modifiable configuration value is equal to the first value.

18. (Original) The method as set forth in Claim 17 further comprising the step of:
in response to a determination that the modifiable configuration value is equal to the first value, executing the misaligned access handling routine.
19. (Original) The method as set forth in Claim 18 further comprising the step of:
in response to a determination that the modifiable configuration value is equal to the second value, determining if the load instruction is speculative.
20. (Original) The method as set forth in Claim 19 further comprising the step of:
in response to a determination that the load instruction is speculative, causing the data processor to dismiss the load instruction.
21. (New) A data processor comprising:
an instruction execution pipeline comprising N processing stages capable of executing a load instruction;
a first status register capable of storing a first modifiable configuration value, said first modifiable configuration value having a first value indicating said data processor is capable of executing an exception handling routine and a second value indicating said data processor is not capable of executing an exception handling routine;

a second status register capable of storing a second modifiable configuration value, said second modifiable configuration value having a first value indicating said load instruction accesses a first region of memory in which an exception cannot be initiated and a second value indicating said load instruction accesses a second region of memory in which an exception can be initiated, said first region of memory including a restricted area of memory or an unrestricted area of memory;

a data protection unit capable of receiving a target address of said load instruction and, in response thereto, setting said second modifiable configuration value to said first value or said second value; and

exception control circuitry capable of determining if said load instruction is speculative, and in response to a determination that said load instruction is speculative, and further in response to a determination that said first modifiable configuration value is equal to said second value and said second modifiable configuration value is equal to said first value, causes said data processor to discuss said load instruction.

22. (New) The data processor as set forth in Claim 21, further comprising:

a misalignment detection circuit capable of determining if said load instruction performs a misaligned access to the target address of said load instruction and, in response to a determination that said load instruction does perform a misaligned access, generating a misalignment

flag, and wherein said exception control circuitry is capable of detecting said misalignment flag and in response thereto determining if said modifiable configuration value is equal to said first value.

23. (New) The data processor as set forth in Claim 22, wherein said exception handling routine is a misaligned access handling routine and wherein said exception control circuitry, in response to a determination that said modifiable configuration value is equal to said first value, causes said data processor to execute said misaligned access handling routine.

24. (New) The data processor as set forth in Claim 23 wherein said exception control circuitry, in response to a determination that said first modifiable configuration value is equal to said second value, and in response to a determination that said load instruction is speculative, causes said data processor to dismiss said load instruction.

25. (New) The data processor as set forth in Claim 24 wherein said data protection unit is further capable of determining if said load instruction accesses a restricted area of memory.

26. (New) The data processor as set forth in Claim 25 wherein said data protection unit, in response to a determination that said load instruction does access a restricted area of memory, and in response to a determination that said second modifiable configuration value is equal to said second value, causes said data processor to execute said exception handling routine.

27. (New) The data processor as set forth in Claim 26 wherein said exception control circuitry, in response to a determination that said load instruction is speculative, and in response to said data protection unit determining that said load instruction does access a restricted area of memory and said second modifiable configuration value is equal to said second value, causes said data processor to dismiss said load instruction.